REMARKS

Applicant concurrently files herewith a Petition and Fee for a Three-Month Extension of Time.

Claims 26-34 are all the claims presently pending in the application. New claims 32-34 have been added to further define the invention. Claims 3-5, 11-18, 20-22, and 24-25 have been canceled without prejudice or disclaimer. Thus, in view of the cancellation of these claims, the prior art rejections are rendered moot.

Applicant gratefully acknowledges the Examiner's indication that claims 26-31 are allowed.

It is noted that the claims have been amended solely to more particularly point out Applicant's invention for the Examiner, and not for distinguishing over the prior art, narrowing the claim in view of the prior art, or for statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached pages are captioned "**Version with markings to show changes made**".

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed by new independent claim 32, is directed to a semiconductor device.

The exemplary semiconductor device includes a pair of first and second transistors, first to third contacts arranged in that order in a first direction, a first gate electrode of the first transistor connected to the first contact and extending in a second direction, a second gate of the second transistor connected to the third contact and extending in the second direction, and a dummy gate electrode extending in the second direction so as to be sandwiched between the

first and second gate electrodes.

A feature of the invention, in an exemplary non-limiting embodiment, is that the first and second gate electrodes and the dummy gate electrode have a same length. This feature exemplarily allows a pair of transistors having the same electric characteristics to be attained, even when a dimensional difference in patterning arises in a manufacturing process. Thus, a pair of transistors are produced to high precision with good manufacturing yield.

An exemplary configuration of the semiconductor device of the invention is shown in Figs. 1-3 of the application.

The conventional structures, such as those discussed below and in the Related Art section of the present application, do not have such a structure, and thus are unable to provide the advantages of the novel structure of the invention.

Indeed, such features are clearly not taught or suggested by the cited references.

II. THE PRIOR ART REFERENCES

Applicant respectfully submits that even if Bush et al. and/or Uehara et al. disclose a dummy electrode, any similarity with the claimed invention ends there. That is, neither Bush nor Uehara et al. teaches or suggests that the first and second gate electrodes and the dummy gate electrode have a same length.

For example, in contrast to the dummy electrode of the present invention as defined by independent claim 32, as shown in Fig. 4, the conductors 40 (e.g., what the Examiner attempts to analogize to the dummy electrodes of the present invention) of Bush et al. do not have the same length as the gate conductors 20 (e.g., what the Examiner attempts to analogize to the gate electrodes of the present invention).

Further, the conductors 40 of Bush et al. are not sandwiched between the gate conductors 20 (e.g., in contrast to the dummy electrode of the present invention as clearly and exemplarily defined by new independent claim 32).

Also, in Bush et al., the conductors 40 are not connected to a contact (e.g., in contrast to the dummy electrode of the present invention as clearly and exemplarily defined by new dependent claim 34).

Uehara is similarly deficient. That is, similarly, as shown in Fig. 5 of Uehara, dummy electrode 50b does not have the same length as the gate electrodes 50a (e.g., in contrast to the dummy electrode of the present invention as defined by independent claim 32).

Further, the dummy electrode 50b does not have the same width as the gate electrodes 50a (e.g., in contrast to the dummy electrode of the present invention as clearly and exemplarily defined by new dependent claim 33). Also, the dummy electrode 50b is not connected to a contact (e.g., in contrast to the dummy electrode of the present invention as clearly and exemplarily defined by new dependent claim 34).

Thus, the structures of Bush et al. and Uehara et al., either alone or even if combined (arguendo), are much different from the claimed invention, and clearly do not teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In response to the Examiner's objection to the Drawings (e.g., on page 2, item 2 of the Office Action), Applicant respectfully notes that the specification has been corrected in the Amendment filed on November 26, 2001 to clearly identify the source diffusion region 7.

In view of the foregoing, Applicant submits that claims 26-34, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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